REMARKS

Reconsideration and allowance of all grounds of objection and rejection, and allowance of all the pending claims are respectfully requested. Claims 1-9 remain pending herein. Claim 1, 6 and 8 are independent claims.

At the outset, Applicant notes with appreciation the indication in the Office Action that claims 6 and 7 recite allowable subject matter. Claim 6 has been rewritten in an independent form including all the recitations of its base claim and intervening claims, thereby placing claims 6 and 7 in immediate condition for allowance.

Replacement sheets for FIGs. 1 and 2 are attached hereto. The drawings now identify all of the enumerated boxes, and support is clearly found throughout the specification. Applicant has also amended claim 1 to show the coupling of the substrate to the power supply reference conductor. No new matter has been added by these changes to the drawings. Reconsideration and withdrawal of this ground of objection is respectfully requested.

Claims 1-3, 8 and 9 stand rejected under 35 U.S.C. §102(b) over Ausserlechner *et al.* (U.S. 6,559,721) (hereafter " Ausserlechner"). Claims 1, 4 and 5 stand rejected under 35 U.S.C. §103(a) over Tanzawa (U.S. Pat. Appn. Pub. No. 2003/0151945) in view of Doyle, III (U.S. 4,710,730). Applicant respectfully traverses these grounds of rejection for the reasons indicated herein below.

Claim 1 has been amended to recite in part that wherein each of the first and second MOS transistors have source-drain diodes in anti-series so that said first and second MOS transistors have a respective maximum breakdown voltage at drain voltages

in mutually opposite directions relative to a substrate voltage, support for which is clearly found at paragraph [0011]. Claim 8 has been similarly amended.

Applicant respectfully submits that independent claims 1 and 8 are clearly not anticipated by Ausserlechner, as this reference is clearly silent with regard to the recitation of a coupling arrangement of drain source diodes of the transistors as claimed.

Applicant strongly disagrees with the statement on page 4 of the Office Action that there is no difference between the drain and source of a MOS transistor; Applicant respectfully submits that there is a difference, and the implication in the Office Action that any configuration reads on the claims as the source and drain are structurally the same is incorrect. The presently claimed invention provides a coupling that (as discussed at least at paragraph [0011]) advantageously eliminates the need to over-dimension any of the transistors relative to the other transistor(s) based on the transistors having breakdown voltages in mutually opposite directions relative to the substrate voltage.

In accordance with MPEP 2131, under 35 U.S.C. §102, according to the United States Court of Appeals for the Federal Circuit, a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference" (*Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (emphasis added)). Therefore, to reject a feature, which is alleged to patentably distinguish the claim containing such feature, as being anticipated by a prior art, the Office Action must establish that the same feature is present in the prior art reference. As Ausserlechner fails to disclose each and every element as set forth in claims 1 and 8, these claims are not anticipated by the reference.

Nor would the recitation of elements, as combined in independent claims 1 and 8, have been obvious at the time of invention as being within the ordinary level of skill in the art (*KSR International v. Teleflex*, 127 S.Ct. 1727, 82 USPQ2d 1385 (2007)).

Applicant also respectfully submits that all claims dependent from one of claims 1 and 8 are not anticipated both because of their dependency from an allowable base claim and because of a separate basis for patentability. Individual consideration for each dependent claim on its won merits is respectfully requested.

Reconsideration and withdrawal of all grounds of rejection under 35 U.S.C. §102(b) are respectfully requested.

With regard to the rejections of claims 1, 4 and 5 under 35 U.S.C. §103(a) over Tanzawa in view of Doyle, Applicant respectfully submits that none of the these claims would have been obvious over the combination of references, at least because the combination of references fails to disclose, suggest or in any other way render obvious the recitation regarding the coupling of the source-drain diodes of the complementary transistors. The claimed invention provides a novel and nonobvious electronic circuit, which advantageously is able to withstand voltages in either direction across its terminals, and which no over-dimensioned transistors are required.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

Aaron Waxler
Registration No. 48,027

Date: May 12, 2008

By: Steve Cha
Attorney for Applicant
Registration No. 44,069

Mail all correspondence to:
Aaron Waxler, Registration No. 48,027
NXP, B.V.
NXP Intellectual Property Department
M/S41-SJ
1109 McKay Drive
San Jose, CA 95131
Phone: (408) 434-3000
Fax: (408) 474-9081